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\* Design Summary \*

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Top Level Output File Name : instruction\_memory.ngc

Primitive and Black Box Usage:

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# BELS : 1

# GND : 1

# IO Buffers : 32

# OBUF : 32

Device utilization summary:

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Selected Device : 6slx9tqg144-3

Slice Logic Utilization:

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 0

Number with an unused Flip Flop: 0 out of 0

Number with an unused LUT: 0 out of 0

Number of fully used LUT-FF pairs: 0 out of 0

Number of unique control sets: 0

IO Utilization:

Number of IOs: 38

Number of bonded IOBs: 32 out of 102 31%

Specific Feature Utilization:

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Cross Clock Domains Report:

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Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 4.26 secs

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Total memory usage is 4506760 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 34 ( 0 filtered)

Number of infos : 0 ( 0 filtered)